REMARKS/ARGUMENTS

This Amendment is being submitted in response to the Office Action dated October 4, 2004. Claims 1-29 are pending. Claims 1, 7 and 15 were amended. Claims 6, 20 and 29 have been canceled as well as previously withdrawn claims 8-14 and 20-28. Accordingly, claims 1-5, 7 and 15-19 remain pending in the present application.

The Examiner rejected claim 29 under 35 USC §102(e) as being anticipated by U.S. Patent No. 6,578,174 to Zizzo. The Examiner rejected claims 1-5, 7, 15-19 and 21 under 35 USC §103(a) as being unpatentable over Zizzo in view of US Patent No. 5,572,712 to Jamal. The Examiner rejected claims 6 and 20 under 35 USC §103(a) as being unpatentable over Zizzo in view of Jamal and further in view of U.S. Patent No. 6,493,855 to Weiss et al.

In response, the limitations of canceled claims 6 and 20 have been incorporated into independent claims 1 and 15, respectively; and claim 7 has been amended to correct a claim dependency.

Applicant agrees with the Examiner's statement made during the rejections of claim 1 and 15 that "Zizzo does not describe the additional elements of providing a request for a memory design that includes BIST, generating the BIST from a user request, and generating a placement and route view of the BIST." The Applicants would go further, however. It is respectfully submitted that insofar as Jamal is directed to a method for creating a BIST HDL on a computer system, a combination of Zizzo and Jamal would result in the system of Zizzo that is also capable of creating a BIST HDL. The combined system would fail to teach or suggest a "method for automatically instantiating BIST modules in memory design" as claimed.

Continuing with the rejection, Applicant also agrees with the Examiner's statement made during the rejections of claims 6 and 20 that neither Zizzo nor Jamal teach the algorithm recited in claims 6 and 20. To cure the defects of Zizzo and Jamal, the Examiner cites Weiss. In contrast to the present invention, however, Weiss discloses a memory architecture for an integrated circuit that is implemented as multiple relatively small sub-arrays of memory that can be arranged around non-memory components, such that the non-memory components do not violate the boundary of the memory component. The sub-arrays may also be arranged in a manner that minimizes the amount of white space in an integrated circuit (Col. 3, lines 1-16).

It is respectfully submitted that nothing in Weiss teaches or suggests a "back-end software process [that] automatically generate(s) a placement and route view of the BIST," as claimed. Weiss discloses a method to arrange the sub-arrays, but fails to teach or suggest the steps of "generating an initial size estimate of an area needed for the memory; allocating a memory having an area of that size; performing placement and routing; and assessing whether the allocated area is sufficient, and if not, incrementing the size of the memory and iterating again, as recited in amended claims 1 and 15. Thus, independent claims 1 and 15 are allowable over combination of Zizzo, Jamal and Weiss.

The arguments above apply with full force and effect to the remaining dependent claims because they are based on allowable independent claims. Therefore, the dependent claims are allowable for at least the same reasons as the independent claims.

In view of the foregoing, it is submitted that claims 1-5, 7 and 15-19 are allowable over the cited references. Because the secondary references stand or fall with the

primary references, claims are allowable because they are dependent upon the allowable independent claims. Accordingly, Applicant respectfully requests reconsideration and passage to issue of claims 1-5, 7 and 15-19 as now presented.

Applicants' attorney believes this application in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,
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Date

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